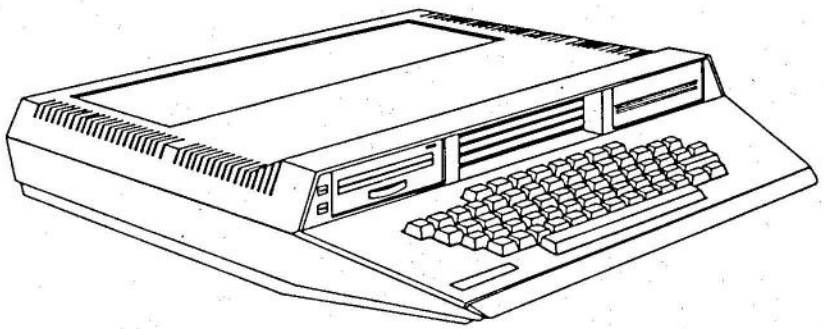
TATUNG

Einstein

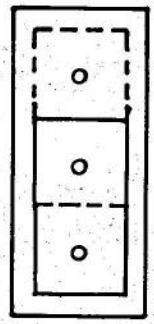
COLOUR MICRO COMPUTER



****
*
TK02 MONOCHROME 80 COLUMN CARD

INSTALLATION & SERVICE INFORMATION
*
****

DEFAULT SELECTOR LINKS

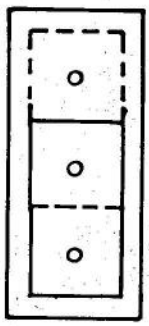


525 line

625 line

FIG. 3. M002

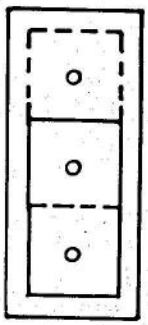
80 column display



Normal output - solid outline

Normal display

FIG. 4. M003



Einstein Standard

International ASCII

FIG. 5. M004

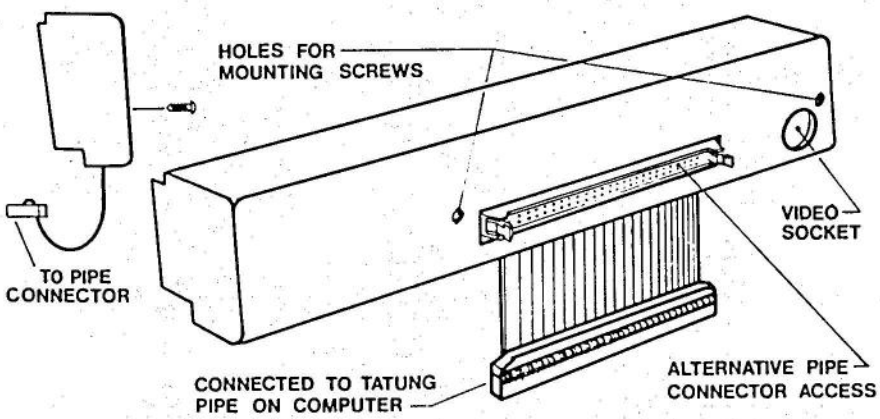

HOLES FOR
MOUNTING SCREWS
VIDEO
SOCKET
TO PIPE
CONNECTOR
CONNECTED TO TATUNG
PIPE ON COMPUTER
ALTERNATIVE PIPE
CONNECTOR ACCESS

FIG. 1.

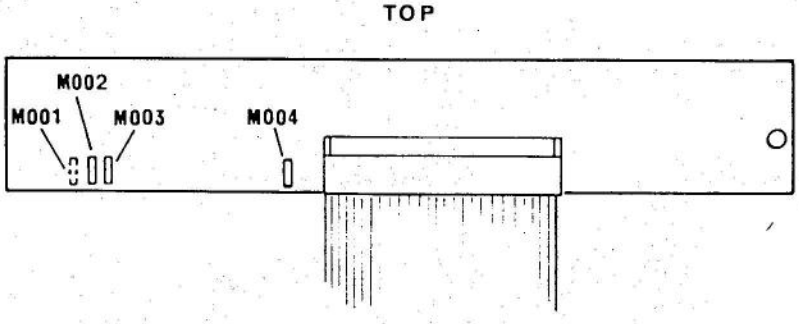

TOP
M002
M001
M003
M004

FIG. 2.

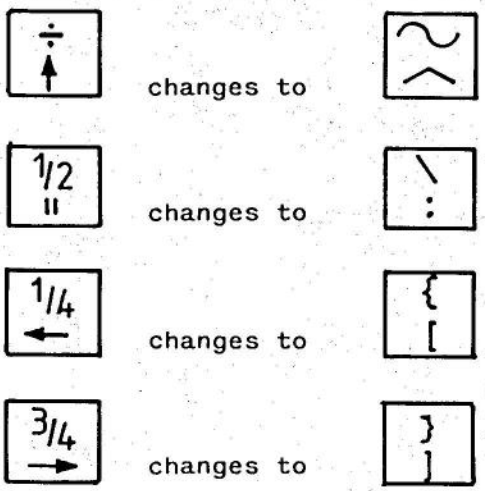


FIG. 6. Character Set changes

HEX VALUE	2	3	4	5	6	7	8	9
0	SP	0	@	P	£	p		
1	!	1	A	Q	a	q		
2	"	2	B	R	b	r		
3	#	3	C	S	c	s		
4	$	4	D	T	d	t		
5	%	5	E	U	e	u		
6	&	6	F	V	f	v		
7	'	7	G	W	g	w		
8	(	8	H	X	h	x		
9	)	9	I	Y	i	y		
A	*	:	J	Z	j	z		
B	+	;	K	[	k	{		
C	,	<	L	\	l	¦		
D	-	=	M	]	m	}		
E	.	>	N	^	n	~		
F	/	?	O	_	o	■		

FIG. 7. Modified ASCII set

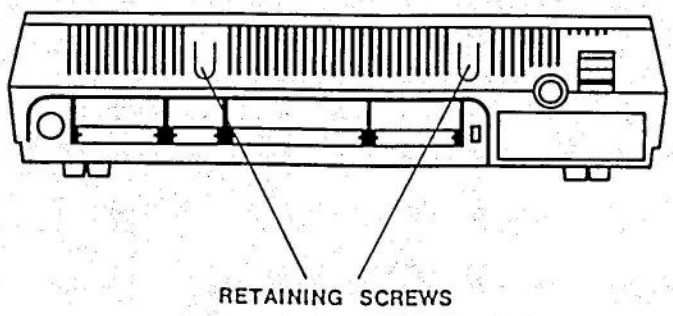


FIG. 8.

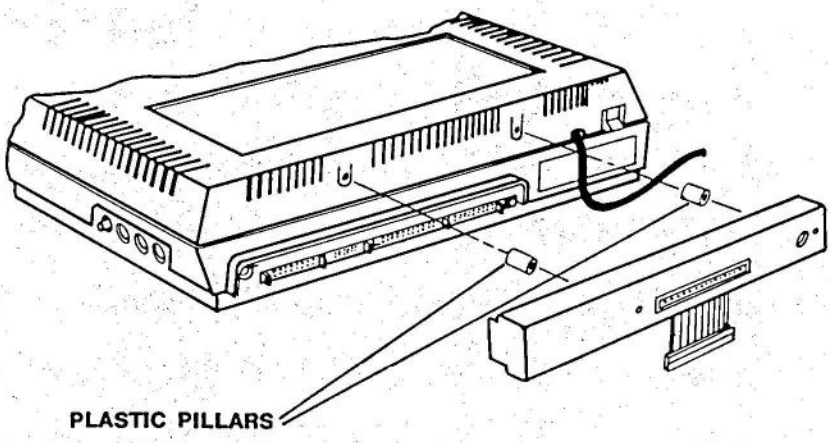


FIG. 9.

PART 1

TK02 MONOCHROME 80 COLUMN CARD

This 80 column card provides the facility for producing an 80 column x 24 line display on a suitable monochrome monitor. An inverse character set (black on white) is available. The unit is secured to the rear of the Einstein computer and connected to the "Tatung Pipe", from where the unit receives power and data. The Pipe is extended to a plug on the rear of the card, to allow for connections to other peripherals were necessary. (See Fig. 1). It may only be used with MOS 1.2 or later.

Before installing the card, there are three selectors which determine its performance according to requirements (See Fig. 2):-

M002 TV Standard

The unit can be used to feed video signals to 525 line 60Hz field format by moving the link to the position covering the top and centre pins. (See Fig. 3) The unit is supplied from the factory in the 625 line 50Hz field position.

M003 Display Status

This sets up the default setting for whichever monitor is in use. There are two conditions:

a) Normal, but 80 column mode selected from keyboard (CTRL P)

b) 80 column, but colour display enabled from keyboard (CTRL N)

The unit is supplied in status (a) from the factory.

Note: Some software will **force** a selection, being configured, say, for 40 column operation. Others may require normal selection from the keyboard.

M004 Character Set

Some programs do not require certain symbols, but require others not available at the keyboard; examples of the 'redundant' characters are ¼,½,¾ etc., while the 'back slash' and 'braces' may be required. The link M004 provides the option for using either the existing Einstein character set, or a modified set. The important changes are seen in Fig. 6, while the link is shown in Fig. 5.

Fitting the unit

1. Remove the retaining screws at the rear of the computer, (See Fig. 8).

2. Ensure the two plastic pillars are inserted into the retaining holes on the TRACK (non component) side of the card. (See Fig. 9).

3. Insert the 60-way connector into the "Pipe" socket, ensuring that the retaining lugs engage.

4. Insert the long screws through the holes in the cover and up through the pillars.

5. Locate the card and cover and GENTLY tighten the screws, securing the cover and card to the rear of the computer cover.

WARNING: DO NOT OVERTIGHTEN

Note: The interconnecting video output cable should be terminated at the computer end in a "Phono" plug. The other end should be of a type suitable for your monitor. The recommended bandwidth for your monitor is 15MHz.

OPERATION

Once the 80 column display has been selected, the computer will respond to the MOS and DOS functions as normal. The 80 column unit will respond to the following:-

HEX VALUE	CONTROL CODE	FUNCTION
01	CTRL - A	Screen dump
04	CTRL - D	Cursor right
06	CTRL - F	Delete character at cursor
07	CTRL - G	Beep
08	CTRL - H	Cursor left
09	CTRL - I	Horizontal tab
0A	CTRL - J	Cursor down
0B	CTRL - K	Cursor up
0C	CTRL - L	Cursor home & clear screen
0D	CTRL - M	Carriage return
0E	CTRL - N	Clear screen 40 column
0F	CTRL - O	Clear screen 32 column
10	CTRL - P	Clear screen 80 column
11	CTRL - Q	Cursor on
12	CTRL - R	Printer on
13	CTRL - S	Printer off
14	CTRL - T	Cursor off
15	CTRL - U	Delete to end of line
16	CTRL - V	Delete to end of screen
17	CTRL - W	Select inverse/normal video
18	CTRL - X	Delete whole line
19	CTRL - Y	Delete to left
1A	CTRL - Z	Insert
1B	CTRL - ↑	Escape
1E	CTRL - ←	Cursor home

PART 2

SERVICING THE TK02

GENERAL

The TK02 consists of a double sided PCB with plated through holes. It is connected to the "Pipe", 60-way IDC 'looped' through to a 60-way IDC plug.

SPECIFICATION

Power Supply:	5V DC +/- 0.25V dc. @ 500mA max.
Interface:	Z80 buffered bus via 60-way IDC socket 'looped' to 60 way plug.
Screen Format:	80 characters x 24 lines, on an 8 x 8 matrix.
Graphics:	Line and block graphics on 8 x 10 matrix. Normal and inverse video capability. Direct cursor addressing capability. 25th 'status' row feature. Link select mode for startup. (80 column or normal)
Character Set:	'Einstein' and (modified) 'ASCII' (Link selected)
Video Standard:	525 line, 60Hz field or 625 line, 50Hz field. Link Selected.
Video Ouput:	Composite video into 75 ohms, @ 1v pk-pk
Video Socket:	Phono type

CIRCUIT DESCRIPTION

The heart of the 80 column unit is the 6845 cathode ray tube controller CRTC (I003). This generates all the memory timing signals and the TV synchronising display and cursor signals. The CRTC is connected to the data bus and resides in the Z80 I/O map at location 48 (Hex) to 4C (Hex). This location is decoded by I016b, (74LS27) I017a, (74LS10) and I007c (74LS32) to provide the $\overline{CS}$ signal. Data is strobed into I003 by $\overline{IORQ}$, inverted by I006a. Address line A0 is connected to the RS input of I003. This arrangement positions the 6845 address register at I/O location 48 (Hex) and the data register at location 49 (Hex).

A 2k x 8 static RAM (I002) is used to store the display data. The address lines for RAM are supplied from either the CRTC or the Z80 bus. The signal source is determined by 3 multiplexers, I013, I014, and I015 (74LS157) which normally route the CRTC address lines to the RAM. The select lines of the multiplexers are controlled by a processor read or write to I/O address 40 to 47 (Hex). This is decoded by I016b (74LS27), I017b (74LS10), I006b (74LS00), and I007b (74LS32). Address lines A0 to A3 are connected to the three most significant address lines of the RAM (via I015) and address lines A8 to A15 are connected to the least significant address lines of the RAM via I013, and I014. The system software uses the Z80 instructions IN r, (C) and OUT (C), (where r is the register ident.), r which places the contents of the C register on address lines A0 to A7 and the contents of the B register on address lines A8 to A15. By using appropriate values in the B register and reading or writing to port 40 (Hex) to 47 (Hex) the full 2k locations of RAM can be accessed. A memory read or write is distinguished by gates I016c (74LS27) and I006c (74LS04) which control the output enable (OE) and input enable (WE) of the RAM. Data is passed to and from the RAM by an octal bi-directional buffer, I001 (74LS245) which is enabled in the direction B to A during a processor write and from A to B during a read operation.

The data output from the RAM (in ASCII form) is passed to the address lines of I004, (2764), which is a character generator ROM. This converts the data bytes into a bit pattern representing the shape of the characters to be displayed on the screen. The row address lines (RA0 to RA3) of the CRTC are used to control the low order address lines of the character generator. These lines count from 0 to 10 and increment by one for each TV line. The count is then reset to zero to begin the next character row.

The bit pattern is then passed to a parallel to serial shift register, I005 (74LS165). The data is loaded into this device when the SH/LD line is taken low. This data is then clocked out in serial form by the 16 MHz signal on pin 2. This is provided by the oscillator formed X001, ½I011 (74S04) and associated components. The serial data output is routed via I008a (74LS86), I009a (74LS20) and I008c (74LS86) to the video buffer stage formed by Q001 and associated components.

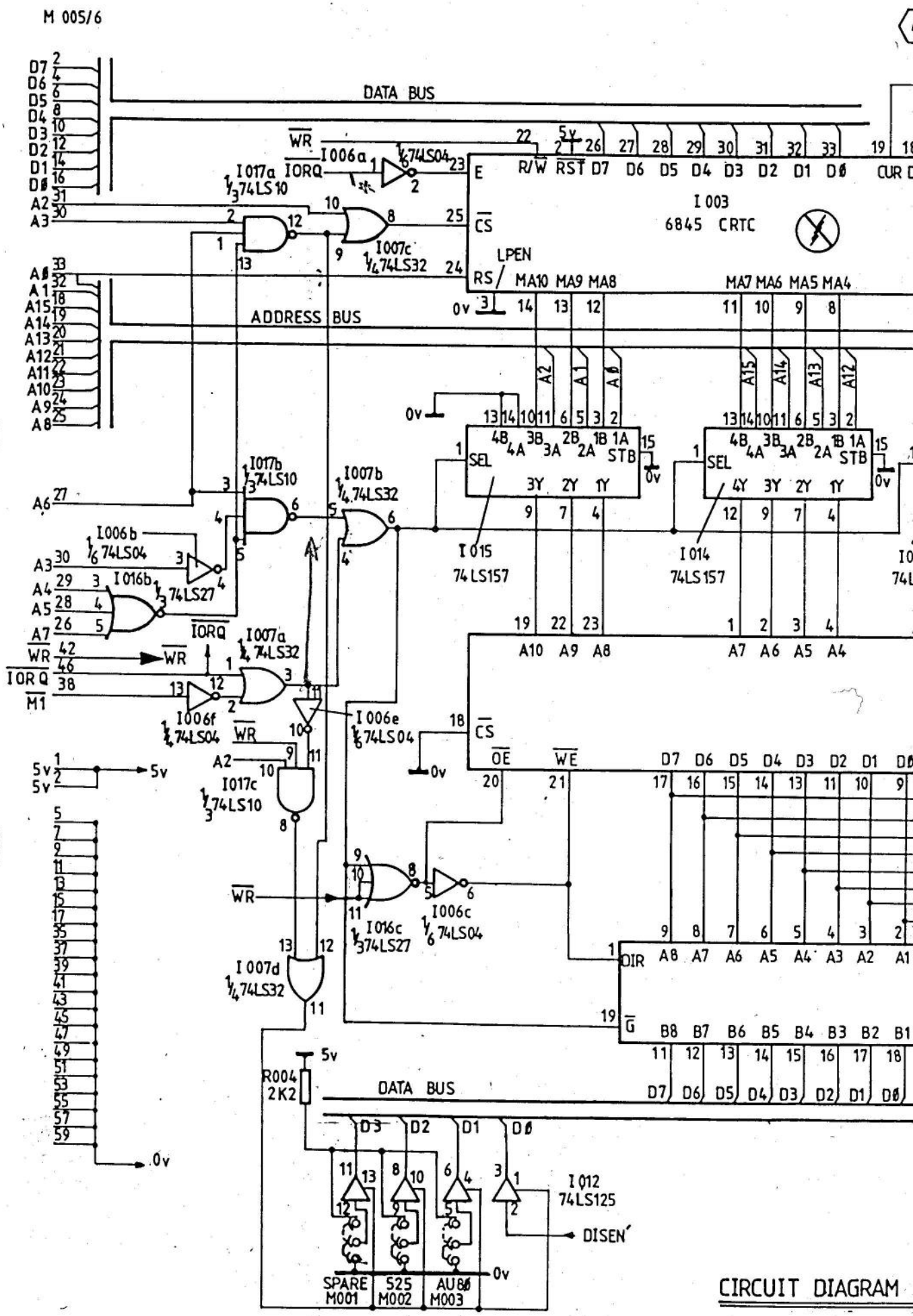
The signal on pin 19 of I003 is active high for the duration of the cursor. This signal is then passed through I018a (74LS74) to retime its position to be co-incident with the start of each character. The latch output (pin 5) is then gated with the video data by I008a which

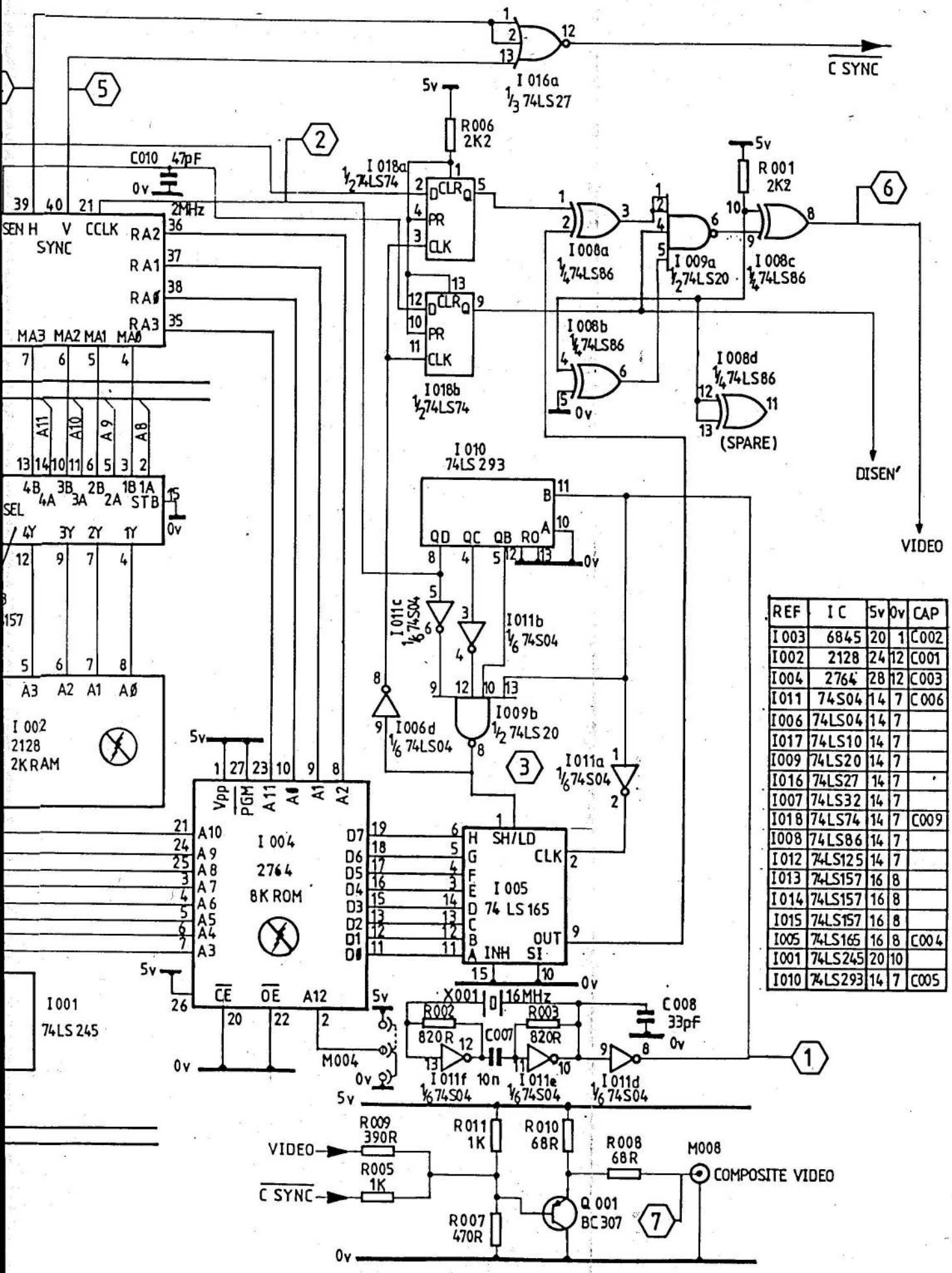
inverts the data from the period of the cursor. The display enable signal on pin 18 of I003 is active high during the display period. This is again retimed by I018b (74LS74) and gated with the video data by I009a (74LS20); so blanking the screen during non display periods.

An input port is provided by I012 (74LS125) which is I/O mapped to location 4C to 4F (Hex). This is decoded by I006f (74LS04), I007 (74LS32), I006e (74LS04), I009b (74LS10) and I007 (74LS32) and is valid only during a processor read operation. Bit 0 of this port is used to enable the processor to test the state of the display enable signal.

Screen disturbance can therefore be avoided by writing to the memory only when the display is not active. i.e. during the line and field blanking periods. Bit 1 of the input port is tested by the software during reset or 'power on' to determine whether the 40 column or 80 column display is enabled. Bit 2 is tested in a similar way to initialise the CRTC to 625 lines, 50 Hz field or 525 line 60Hz field. Bit 3 is reserved for possible future expansion.

M 005/6


DATA BUS
ADDRESS BUS
I 003
6845 CRTC
I 015
74LS157
I 014
74LS157
I017a
I017b
I017c
I007a
I007b
I007c
I007d
I006a
I006b
I006c
I006e
I006f
I016b
I016c
R004
2K2
I 012
74LS125
DISEN
SPARE
M001
525
M002
AU8Ø
M003
CIRCUIT DIAGRAM

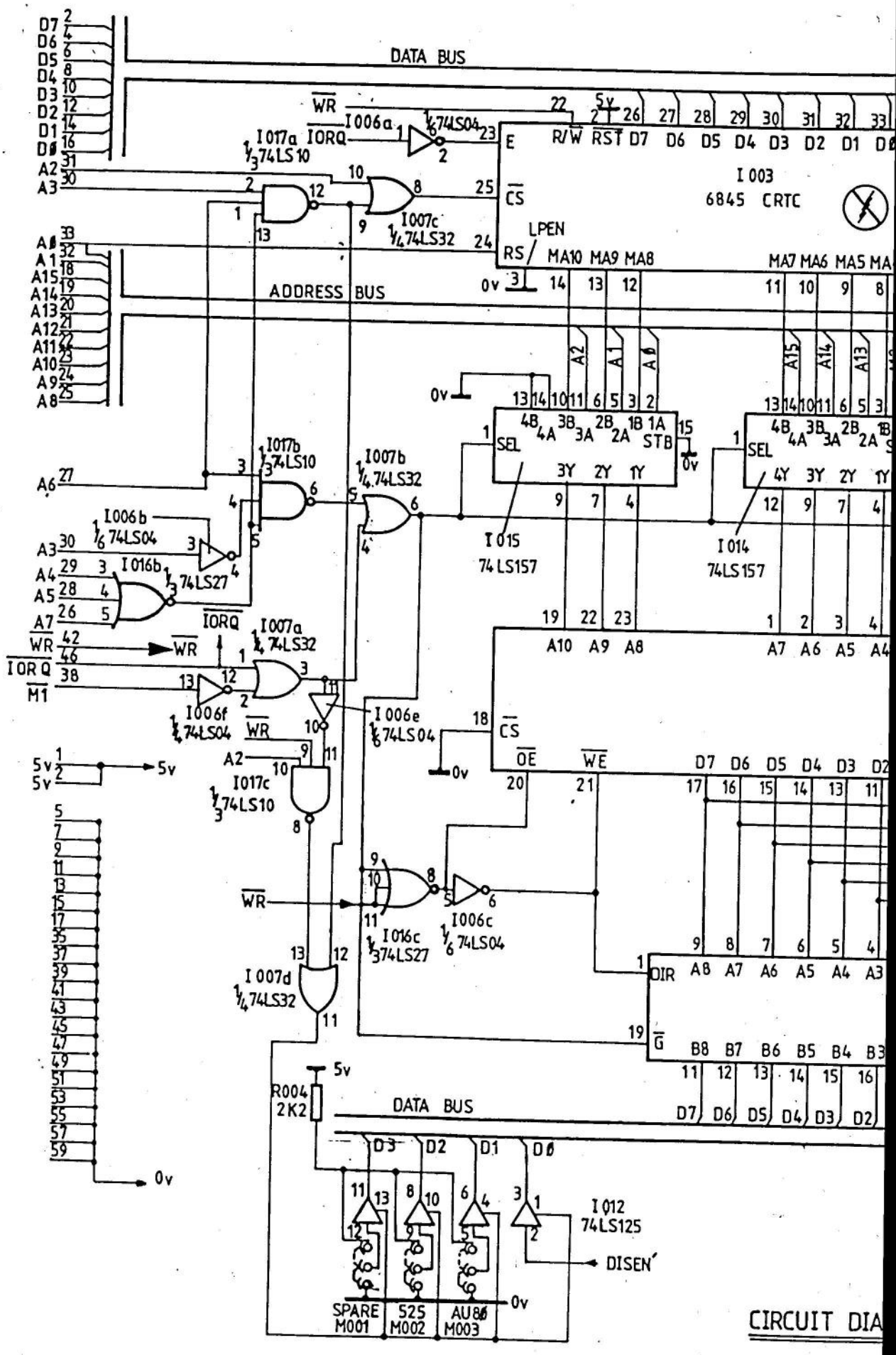


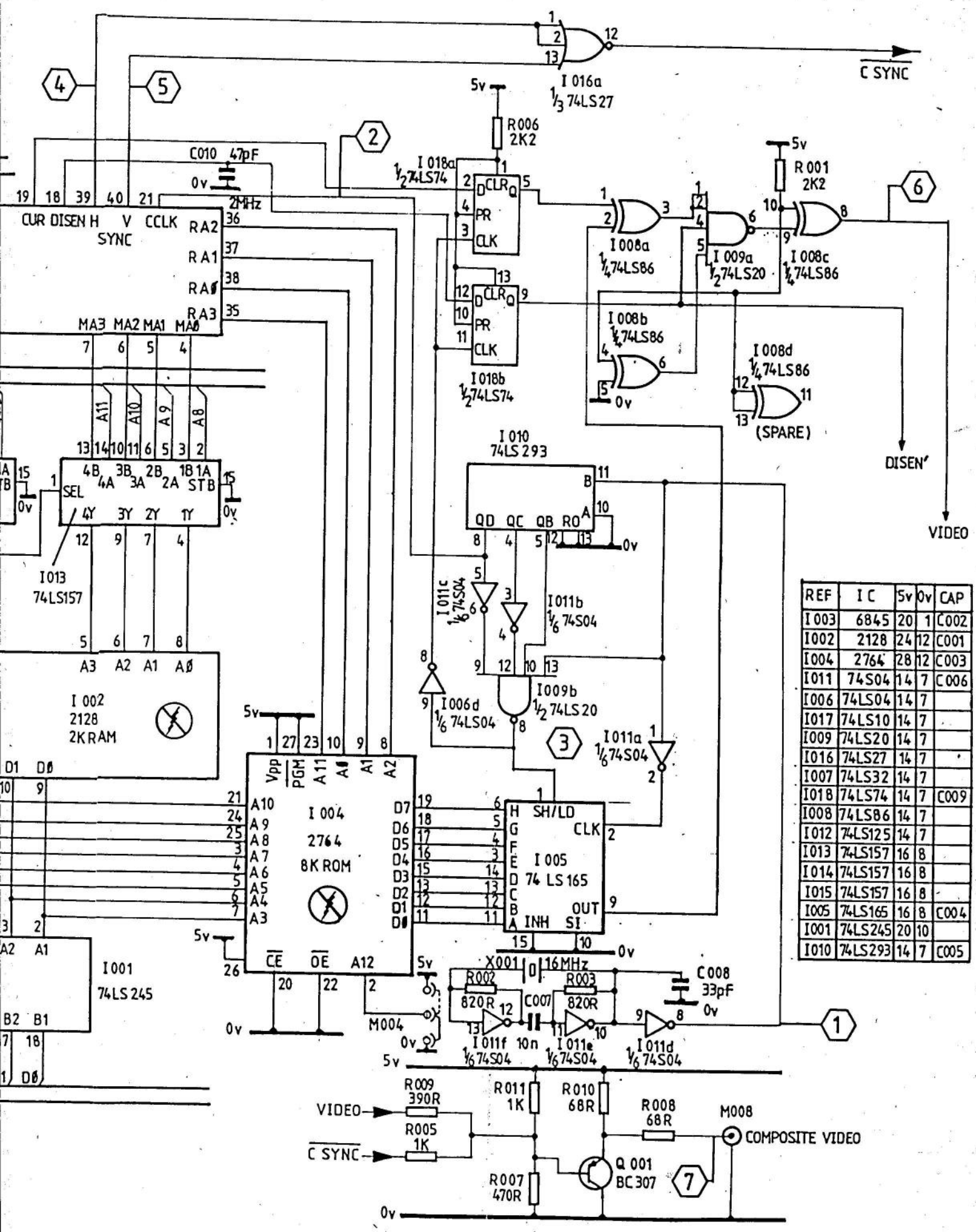
REF	IC	5v	0v	CAP
I 003	6845	20	1	C002
I002	2128	24	12	C001
I004	2764	28	12	C003
I011	74S04	14	7	C006
I006	74LS04	14	7	
I017	74LS10	14	7	
I009	74LS20	14	7	
I016	74LS27	14	7	
I007	74LS32	14	7	
I018	74LS74	14	7	C009
I008	74LS86	14	7	
I012	74LS125	14	7	
I013	74LS157	16	8	
I014	74LS157	16	8	
I015	74LS157	16	8	
I005	74LS165	16	8	C004
I001	74LS245	20	10	
I010	74LS293	14	7	C005

80 COLUMN MONOCHROME CARD

DRG No 83 1601 5 Iss 1

M 005/6


DATA BUS
ADDRESS BUS
I 003
6845 CRTC
I 015
74LS157
I 014
74LS157
I 012
74LS125
DISEN'
R004
2K2
SPARE
M001
S25
M002
AU80
M003
CIRCUIT DIA



REF	I C	5v	0v	CAP
I 003	6845	20	1	C002
I002	2128	24	12	C001
I004	2764	28	12	C003
I011	74S04	14	7	C006
I006	74LS04	14	7	
I017	74LS10	14	7	
I009	74LS20	14	7	
I016	74LS27	14	7	
I007	74LS32	14	7	
I018	74LS74	14	7	C009
I008	74LS86	14	7	
I012	74LS125	14	7	
I013	74LS157	16	8	
I014	74LS157	16	8	
I015	74LS157	16	8	
I005	74LS165	16	8	C004
I001	74LS245	20	10	
I010	74LS293	14	7	C005

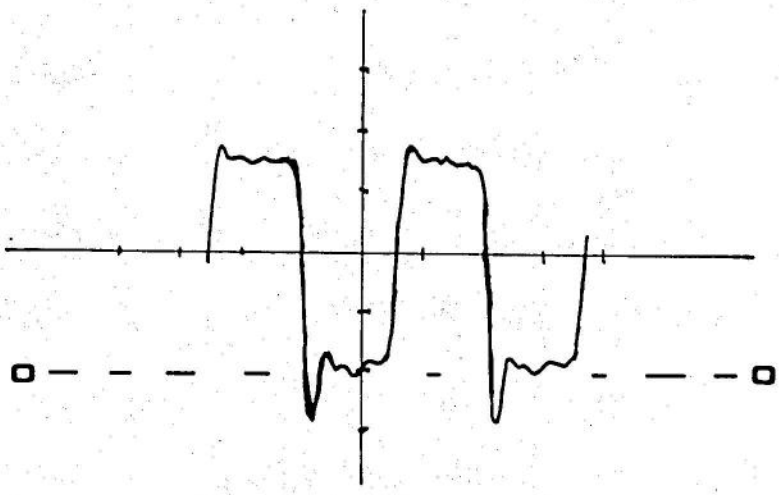
RAM 80 COLUMN MONOCHROME CARD

DRG No 83 1601 5 Iss 1

W A V E F O R M S

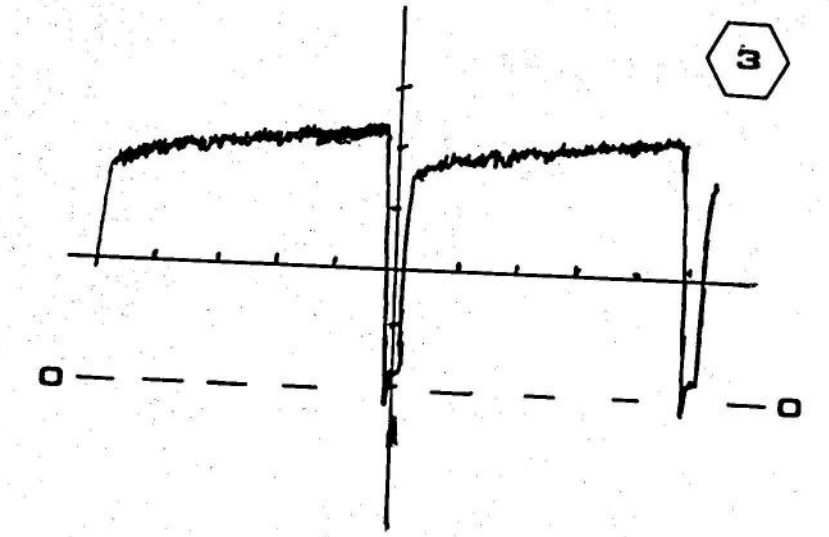
The 16MHz Clock

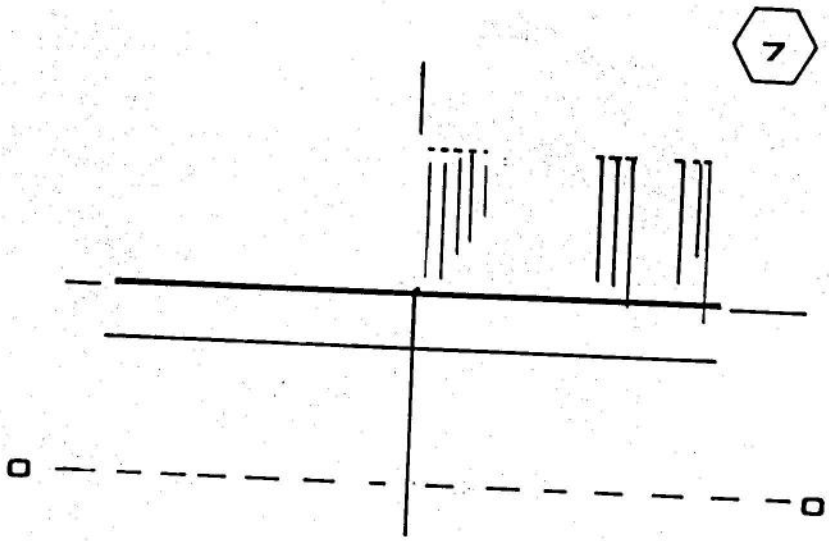
1



2

WAVEFORMS

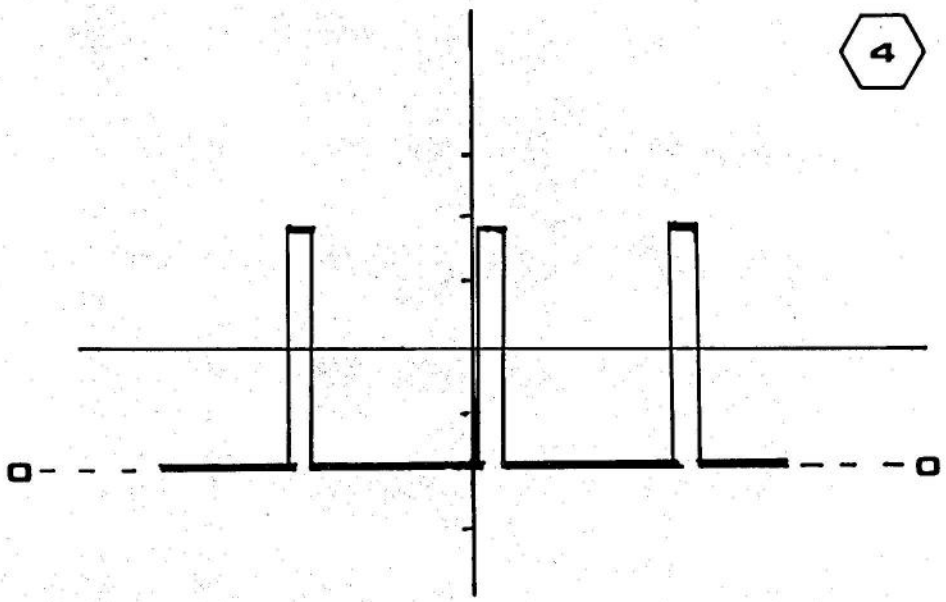




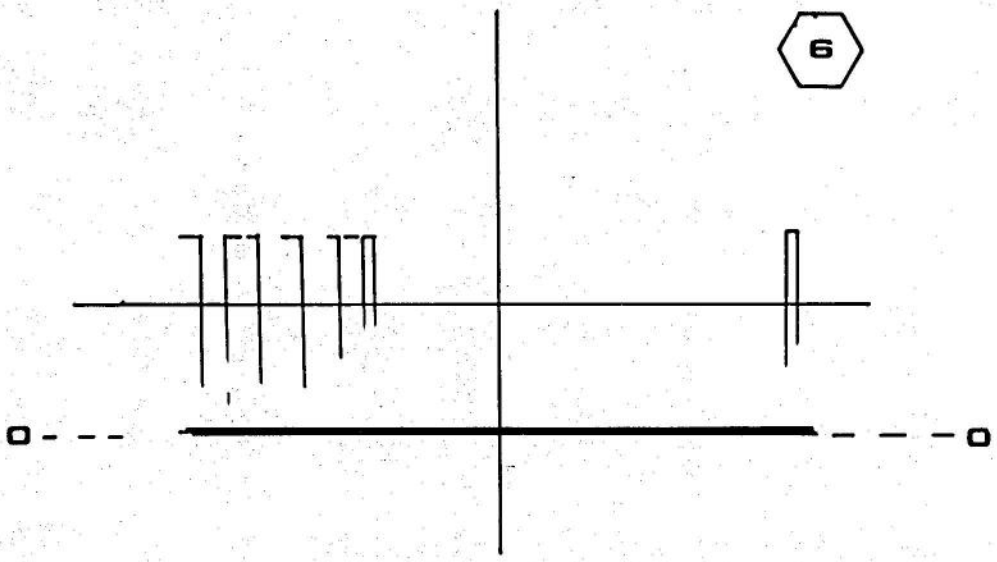
Note: Some waveforms will be "condition dependant", and thus may change. '0' indicates the zero volt (ground) position of the trace.

WAVEFORMS

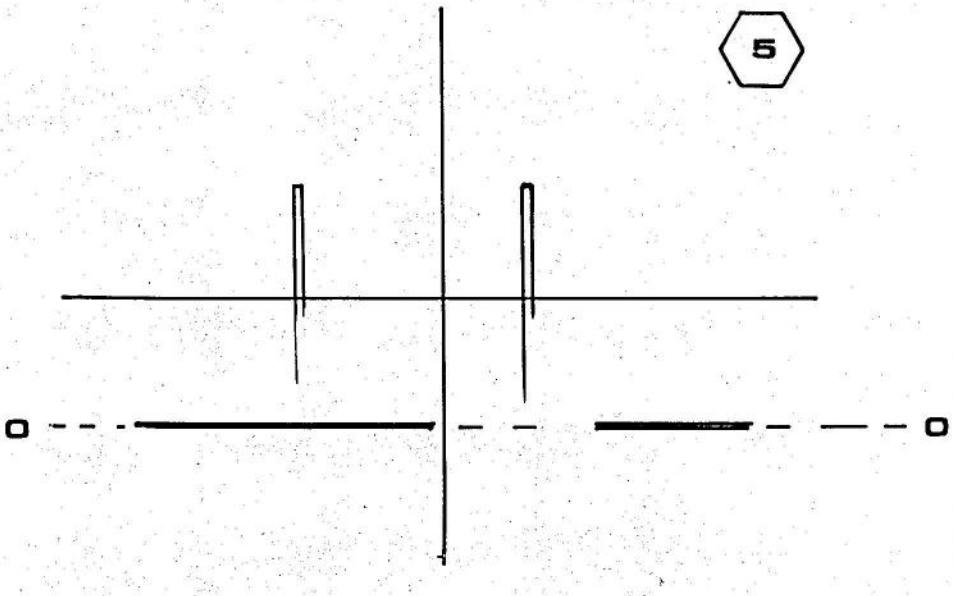
4



6



5



TATUNG BILL OF MATERIAL

LOCATION Bradford

MODEL Nº.

ASSEMBLY PCB 80 Column Mono Unit (Axial Insert) ASS'Y Nº. 05-2408-5/A EDITION 2

part nº.	per	description		circuit ref	issue	co
85-4446-8	1	PWB 80 Column mono unit				
11-4188-0	2	Res 68R 0.25W 5% C-Film	TS871 J11	R008,010		
11-2741-1	1	Res 390R 0.25W 5% C-Film	TS871 J11	R009		
11-3172-9	1	Res 470R 0.25W 5% C-Film	TS871 J11	R007		
11-3184-2	2	Res 820R 0.25W 5% C-Film	TS871 J11	R002,003		
11-2731-4	2	Res 1K 0.25W 5% C-Film	TS871 J11	R005,011		
11-2732-2	3	Res 2K2 0.25W 5% C-Film	TS871 J11	R001,4,6		
14-6355-1	1	Cap 33P 5% 50V Cer Tub	TS882 W14	C008		
14-6359-4	1	Cap 10n 20% 25V Cer Tub	TS882 W14	C007		
14-6794-8	7	Cap 100n $^{+80}_{-20}$% 50V Multilayer Cer	PCL 8-04-09	C001,2,3 4,5,6,9		

LOCATION Bradford

SHEET 1 OF 1

MODEL Nº.

ASSEMBLY PCB 80-Column Mono Unit (Hand Insert) ASS'Y Nº. 05-2408-5/H EDITION 2

part nº.	per	description	circuit ref	issue	c
05-2408-5/A	One	PCB 80 Column Mono Unit			
14-3816-6	1	Capacitor 470pf 10% 50V Ceramic TS882 N14	C010	3,	
19-8187-0	1	Int Circuit SY6845S SYNERTEC PCL1-17-10	I003	1,	
19-8170-6	1	Int. Cct SY2128-1 PCL1-17-02	I002		
19-8097-1/PG02	1	Int Cct To Spec 85-9702-2	I004	3,	
19-8171-4	1	Int Cct 74S04 PCL1-17-03	I011		
19-7990-6	1	Int Cct 74LS04 PCL1-04-09	I006		
19-8172-2	1	Int. Cct 74LS10 PCL1-17-04	I017		
19-8173-0	1	Int. Cct 74LS20 PCL1-17-05	I009		
19-8174-9	1	Int. Cct 74LS27 PCL1-17-06	I016		
18-2182-2	1	Int. Cct 74LS32 PCL1-14-09	I007		
19-8007-6	1	Int. Cct 74LS74 PCL1-15-01	I018		
19-8008-4	1	Int. Cct 74LS86 PCL1-16-06	I008		
19-8175-7	1	Int. Cct 74LS125 PCL1-17-07	I012		
19-4867-9	3	Int. Cct 74LS157 PCL1-14-10	I013,14, 15,		
19-8176-5	1	Int. Cct 74LS165 PCL1-17-08	I005		
19-8091-2	1	Int. Cct 74LS245 PCL1-11-09	I001		
19-8023-8	1	Int. Cct 74LS293 PCL1-07-07	I010		
25-1772-8	1	I.C. Mounting socket 24-way	I002A	1,	
25-2017-6	1	I.C. Mounting Socket 28-way	I004A		
25-1936-4	1	I.C. Mounting Socket 40-way	I003A	1,	
22-8076-0	3	Connector 3 way plug 22-03-2031 Molex	M002,3,4		
22-8077-9	3	Connector 2 way shunt 15-38-1024 Molex	M002A, 3A, 4A		
19-5782-1	1	Transistor Gen Purpose PNP TS865 AF19	Q001		
05-2409-3	One	Wiring Harness 80-Column Mono Unit			
16-1905-5	1	Crystal 16MHz (30pF load cap) PCL9-04-09	X001		
22-8116-3	1	Conn 60 way plug M52-1260-260 Flexicon	M005		
41-1305-5	2	Screw T/F Stl Rec Pn Hd B No. 4x1/4 TS710 VD41		2,	
22-8120-1	1	Socket Phono SQ.3063 S.M.K.	M008		
32-0589-4	12.5 mm	Wire Tinned Copper 23 swg BS128 1 Link Pref 2.5mm	J001	1,	
32-0589-4	30 mm	Wire Tinned Copper 23 swg BS128 1 Link Pref 11.5mm	X001M	3,	

issue nº.	1	2	3	4	5	6	7	8	compiled